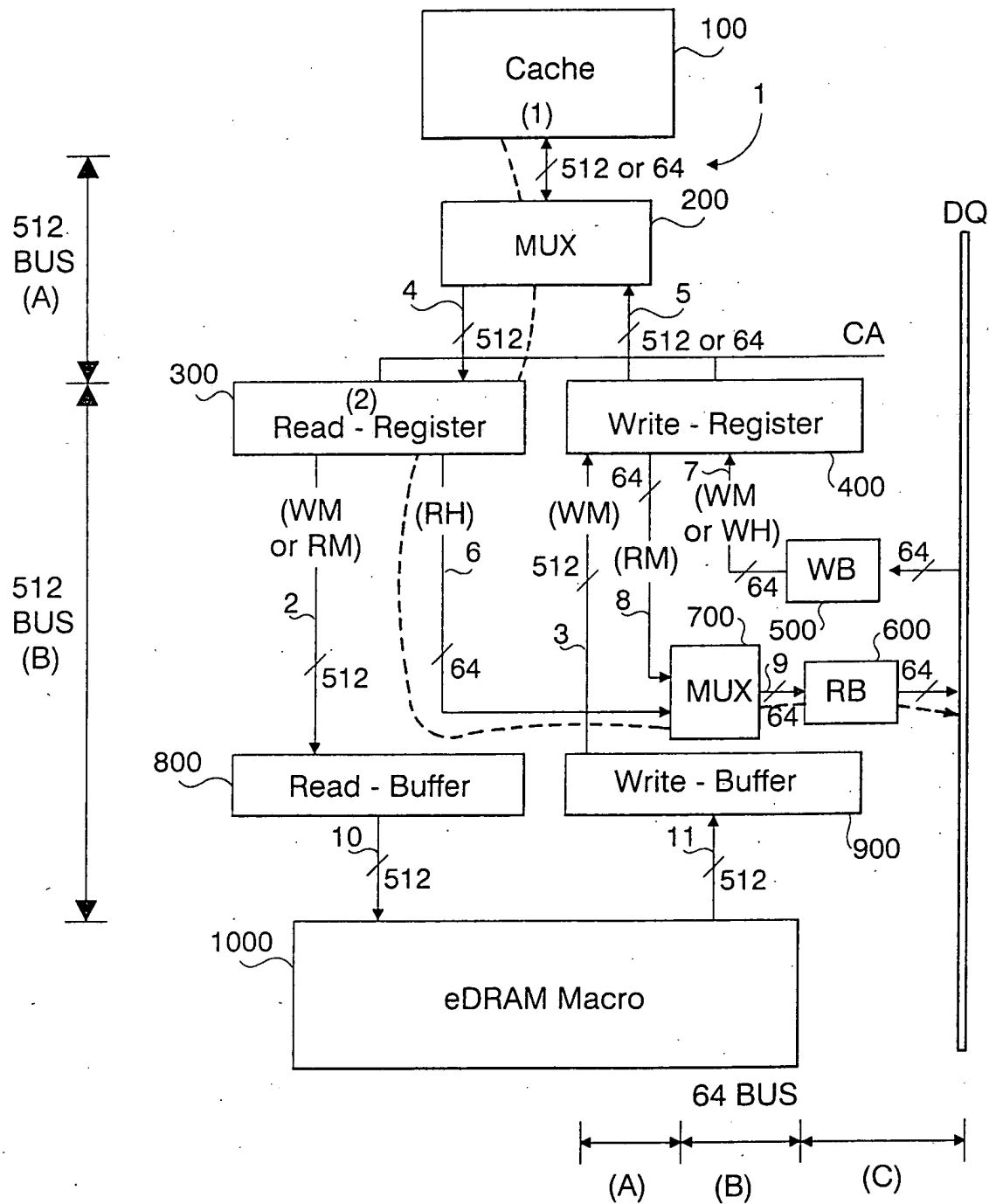




Figure 1

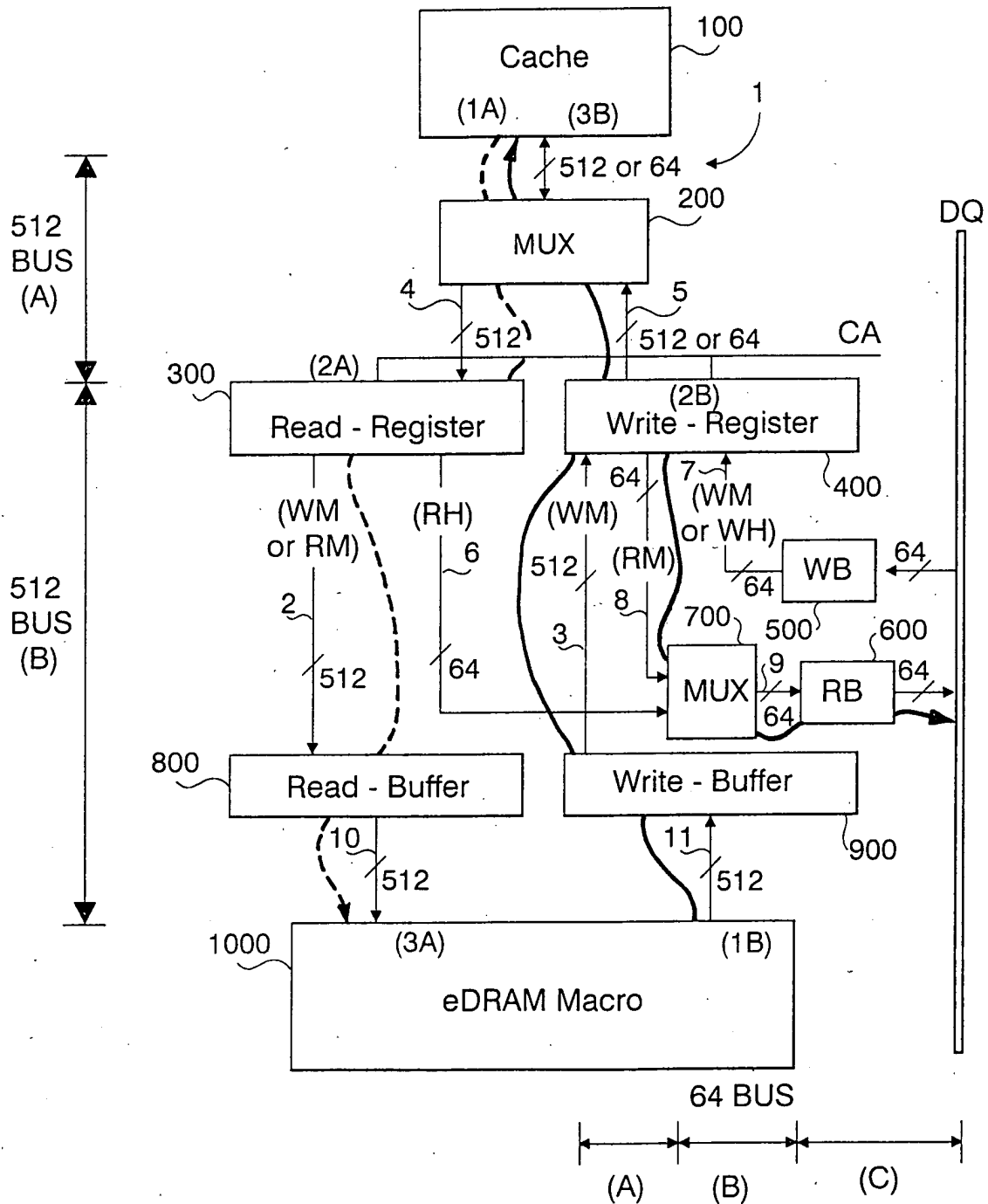


Two-Cycle Read Hit Data Path

Figure 2

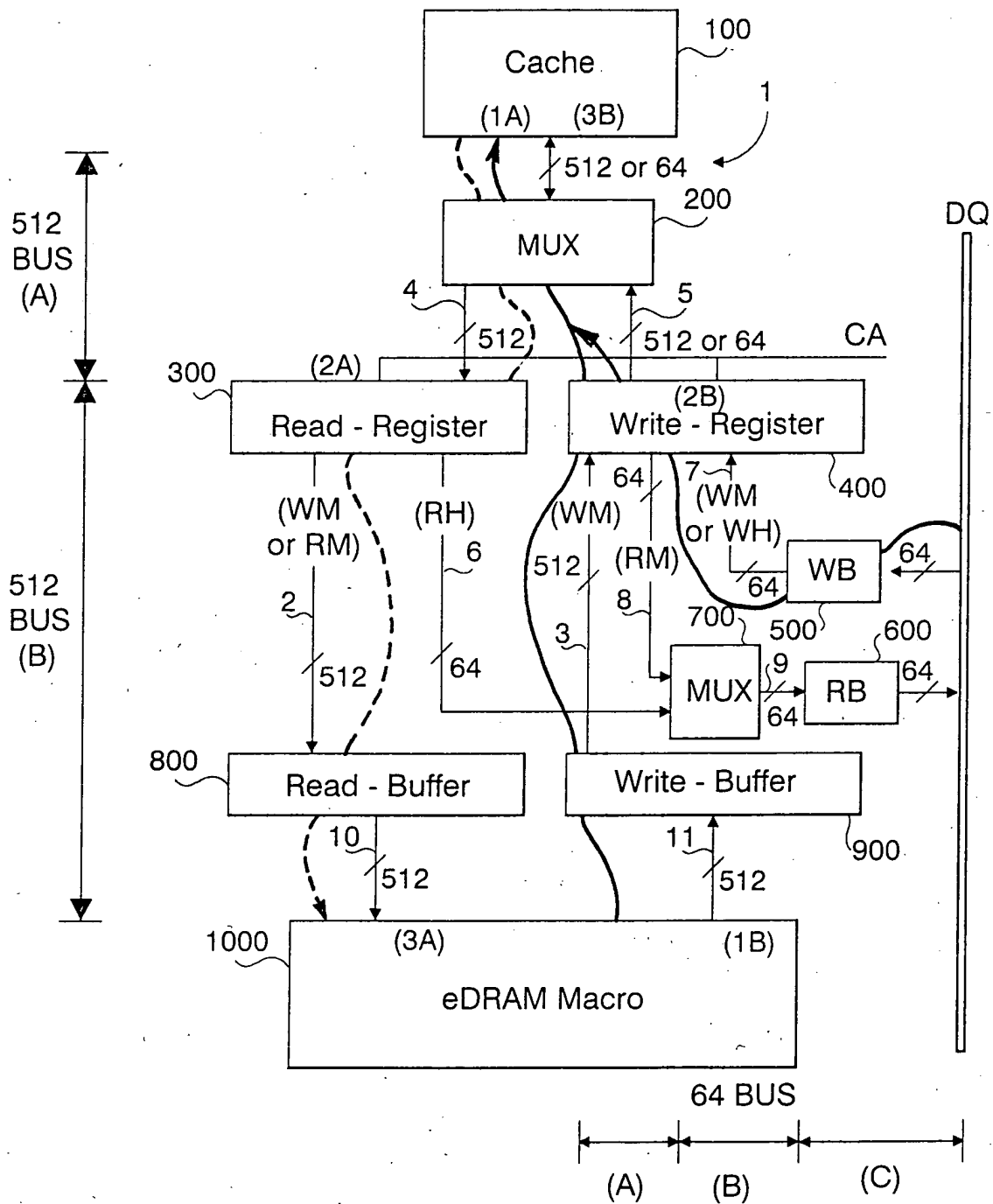


Figure 3



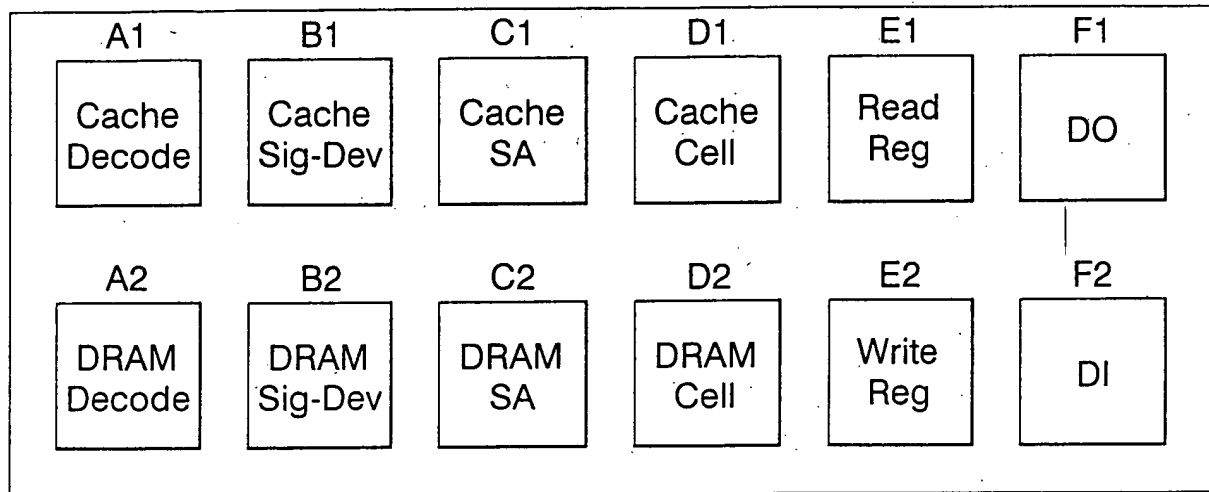
Three-Cycle Read Miss Data Path

Figure 4

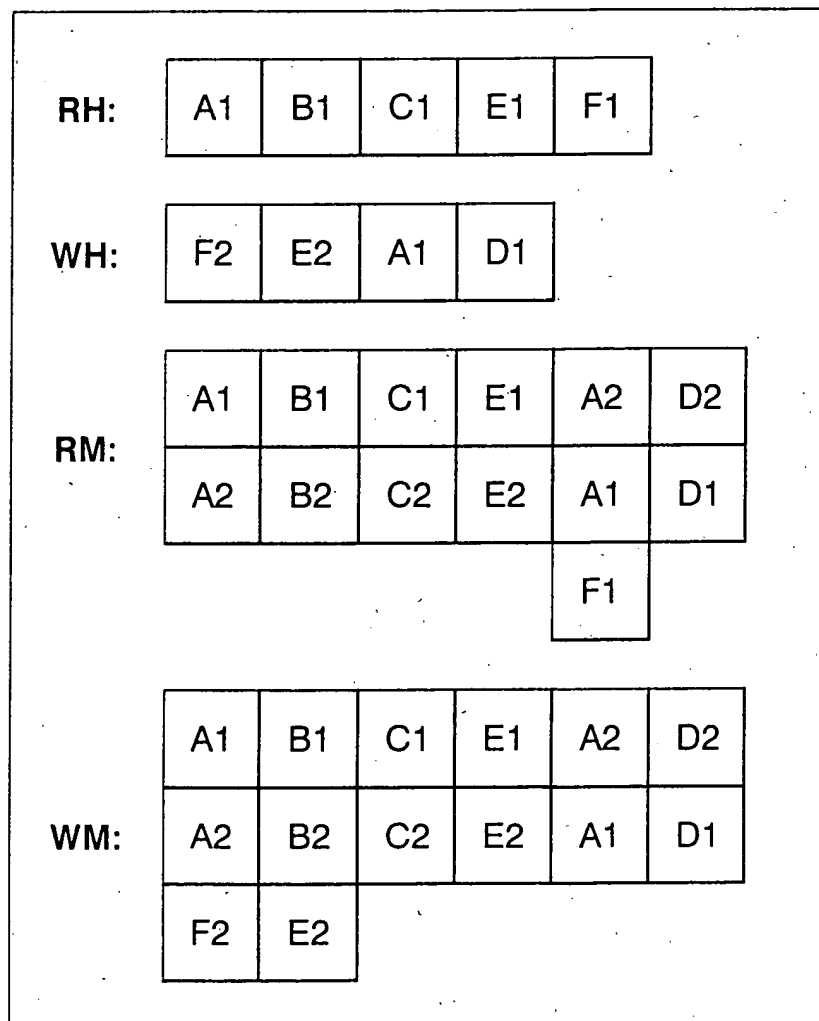


Three-Cycle Write Miss Data Path

Figure 5

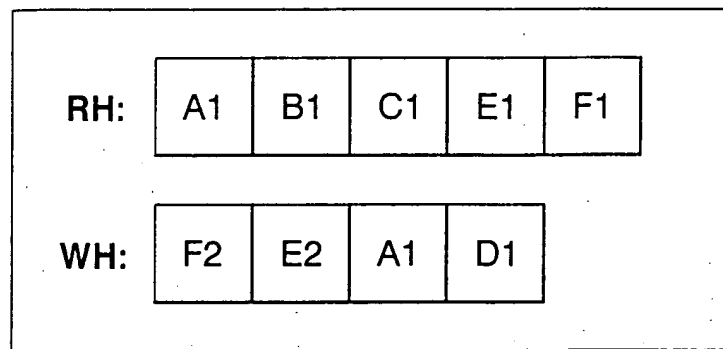


Pipe Operation Code

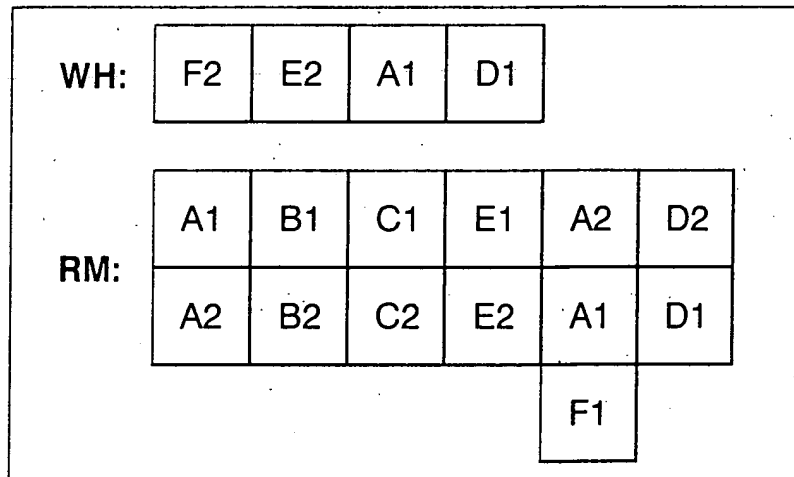
Figure 6

Read/Write Pipeline Sequences

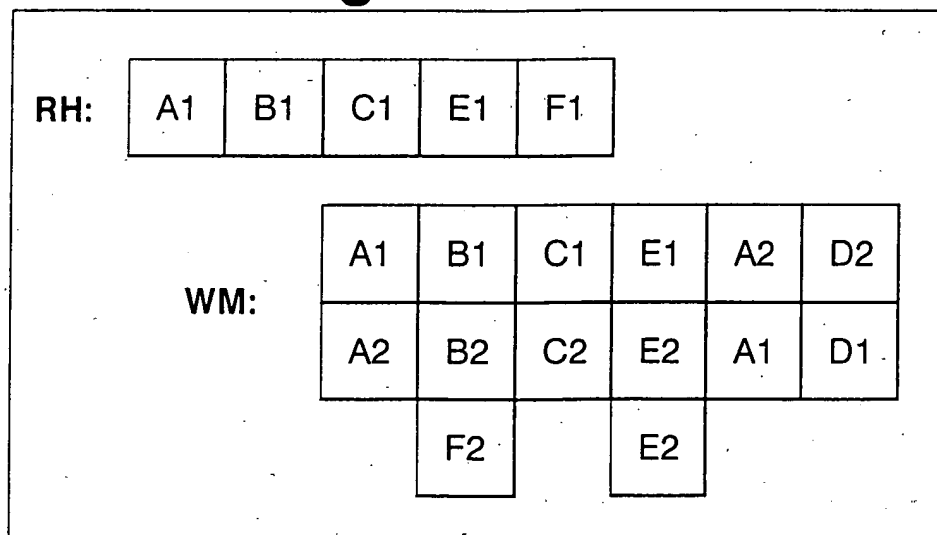
Figure 7



Parallel RH and WH Operations

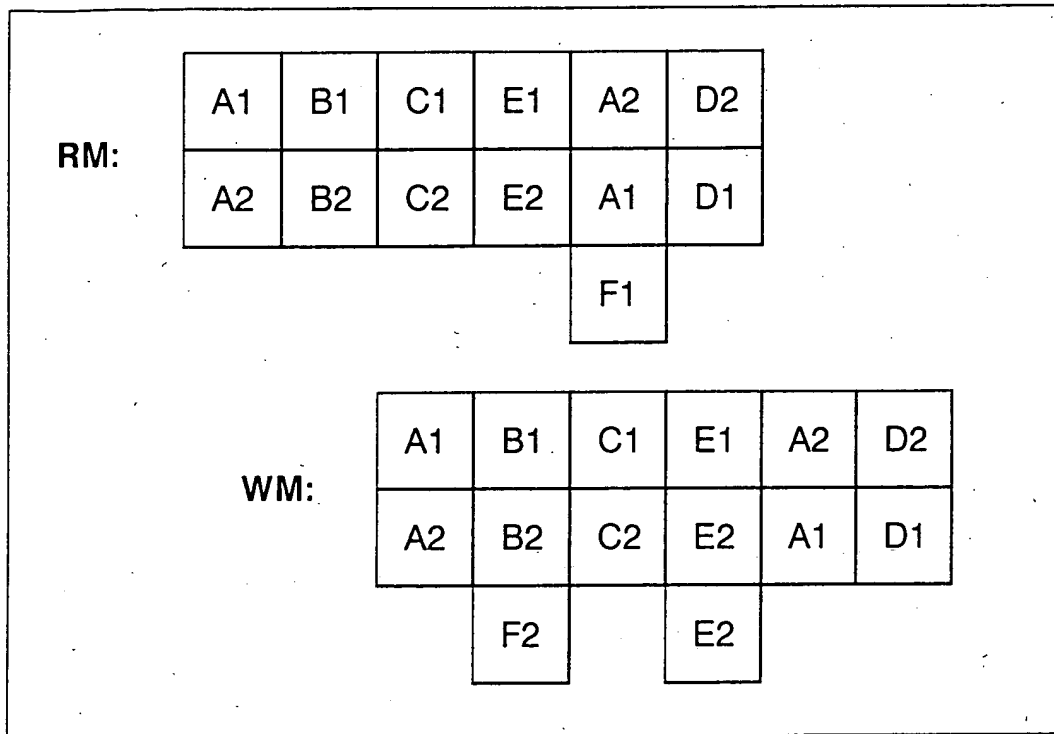
Figure 8-1

Parallel WH and RM Operations

Figure 8-2

Parallel RH and WM Operations

Figure 8-3



Parallel RM and WM Operations

Figure 8-4

	RH	RM	WH	WM	
RH	2	2	0	2	Pipe Delay
RM	2	2	0	2	
WH	0	0	2	0	
WM	2	2	0	2	

Possible Operation Sequence and Delay

Figure 9